

File

2/8

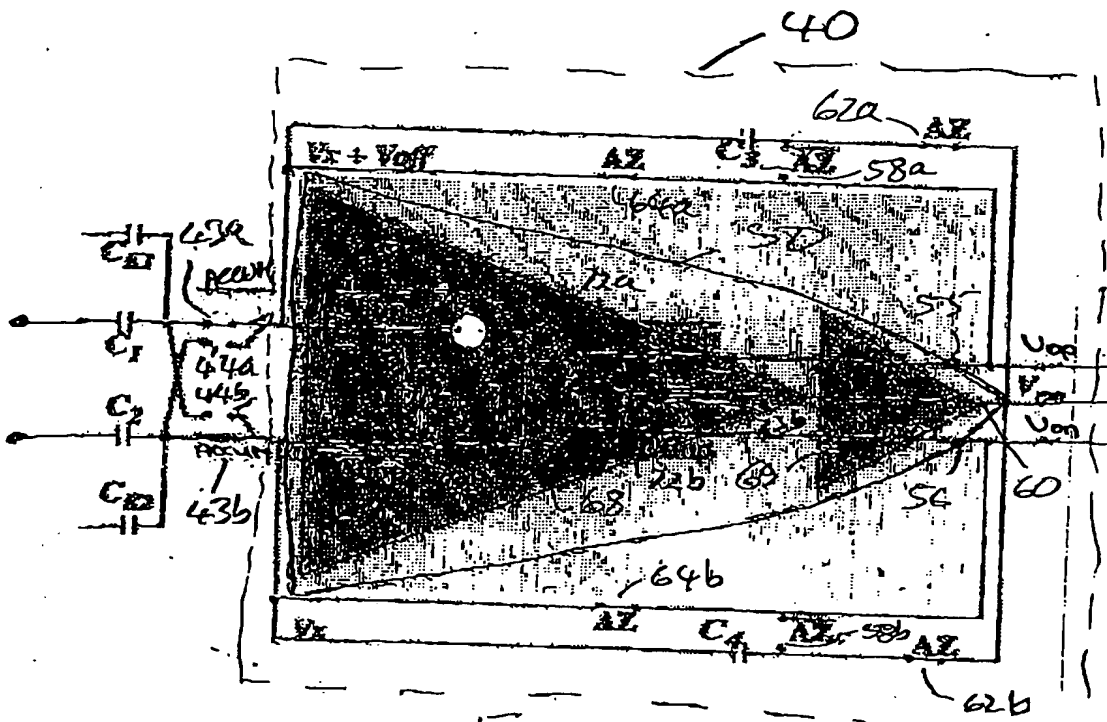


FIG 2

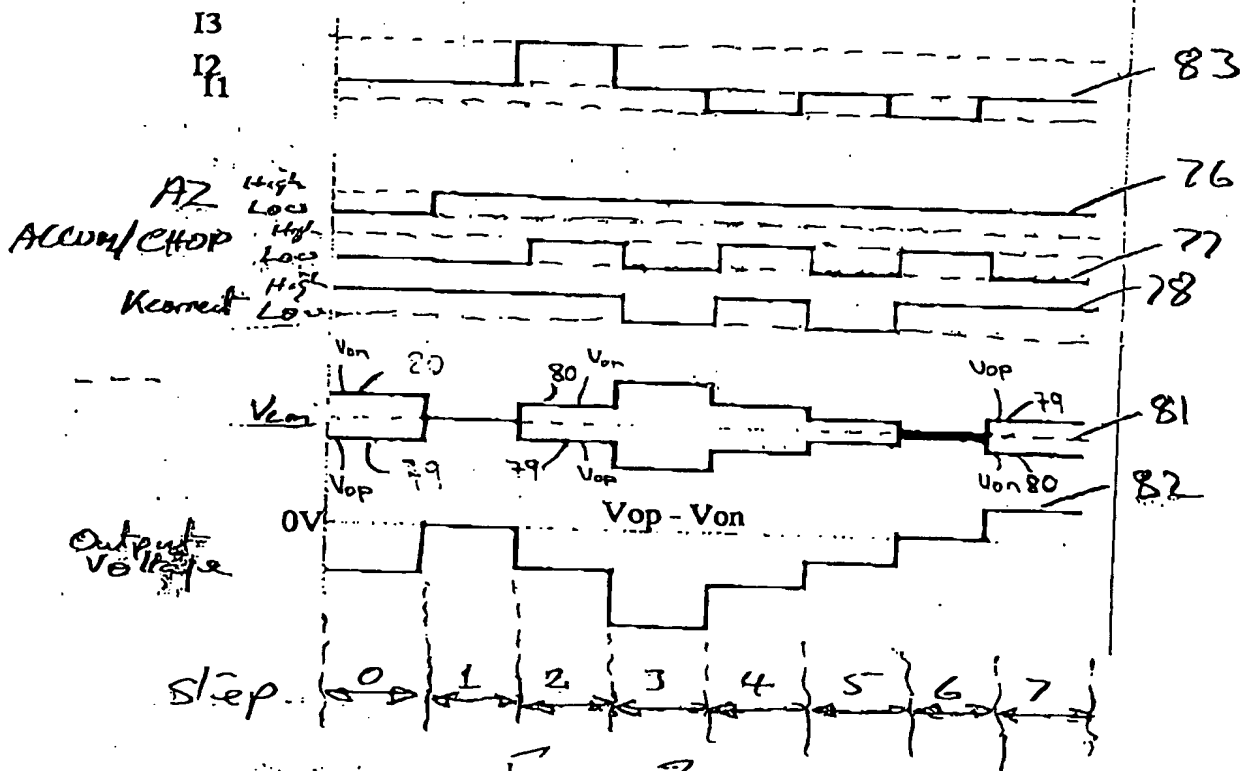
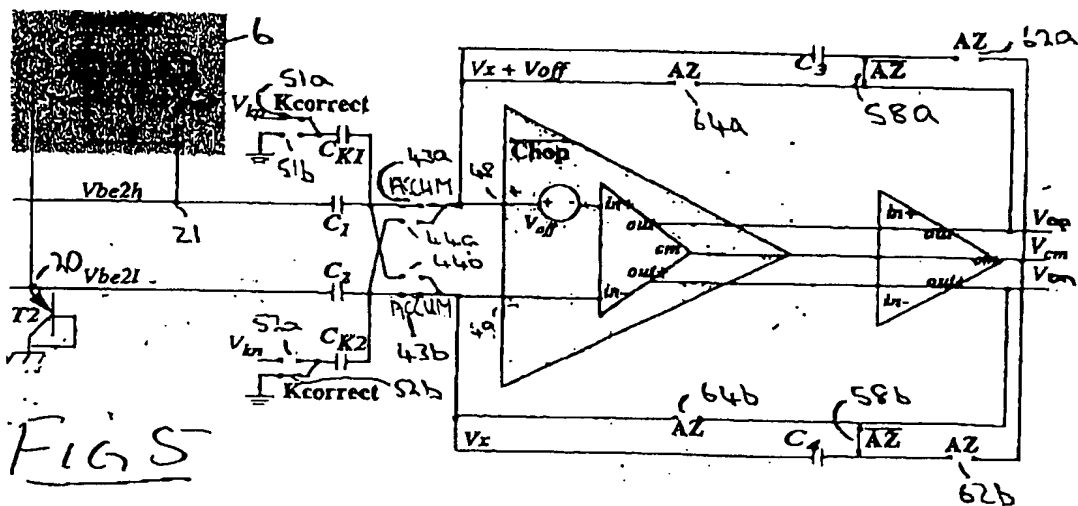


FIG 3

The diagram shows a two-stage CMOS differential amplifier. The first stage is a differential pair with NMOS transistors 43a and 43b, and PMOS load transistors 44a and 44b. The gates of 43a and 43b are connected to a common-mode feedback node 48, which is the output of a second-stage differential pair 58a and 58b. The gates of 44a and 44b are connected to a common-mode feedback node 49, which is the output of the first stage. The inputs of the first stage are connected to a differential-mode input 20 and a common-mode input 21. The outputs of the first stage are connected to a differential-mode output 22 and a common-mode output 23. The circuit includes various biasing and feedback components, including resistors \$R_{correct}\$, capacitors \$C_1, C_2, C_3, C_4\$, and a feedback loop 74.

FIG 4



FIGS

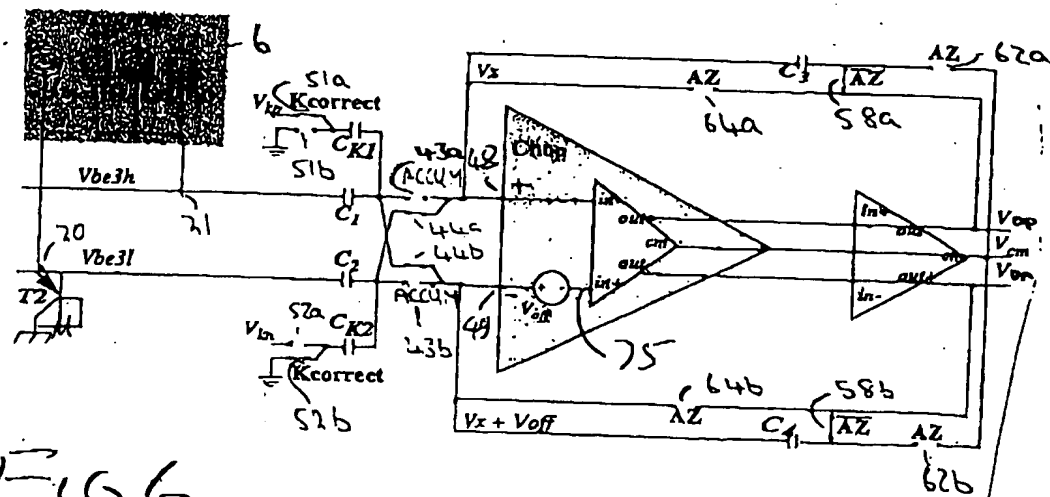


Fig 6

Fig 7

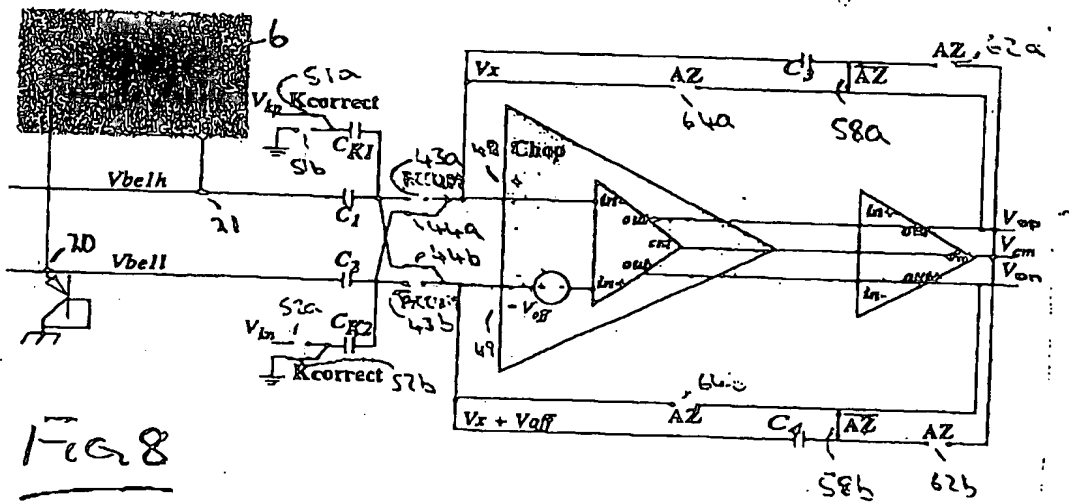
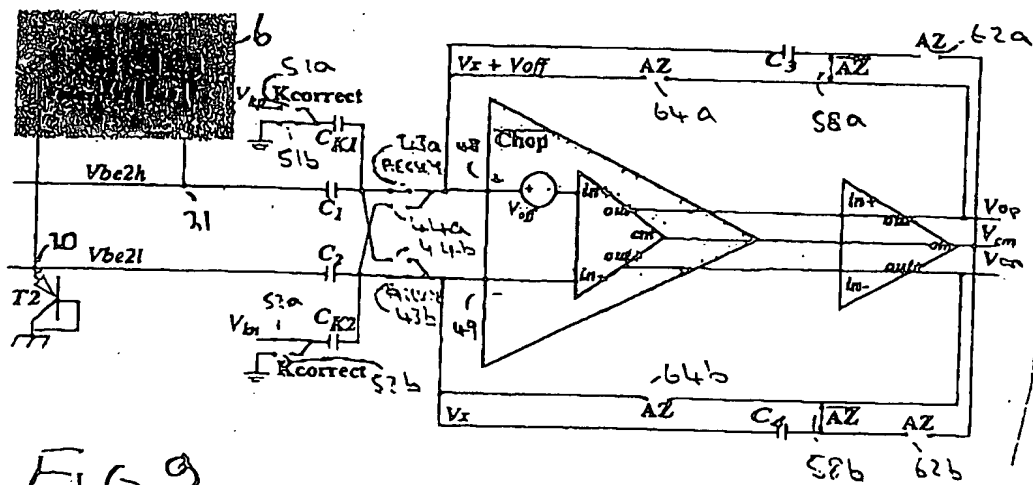


Fig 8



F G 9

FIG 10

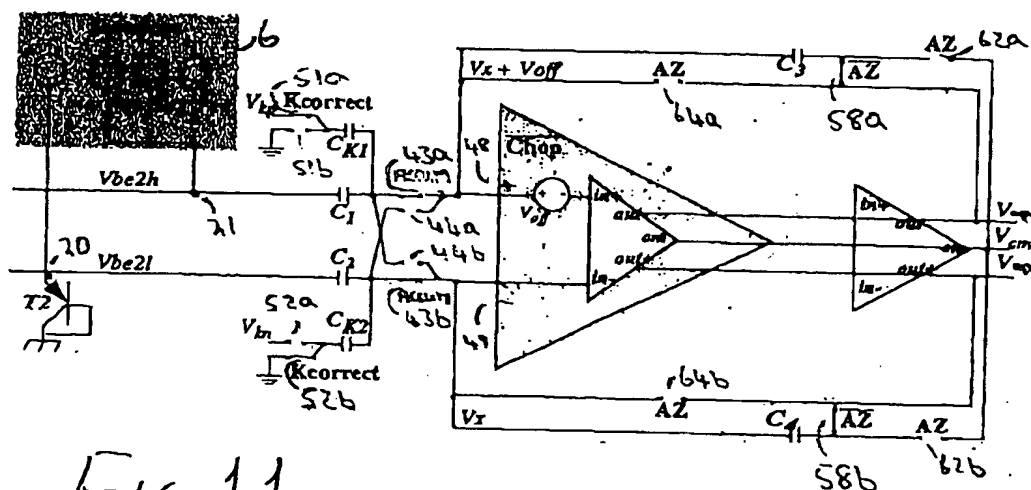
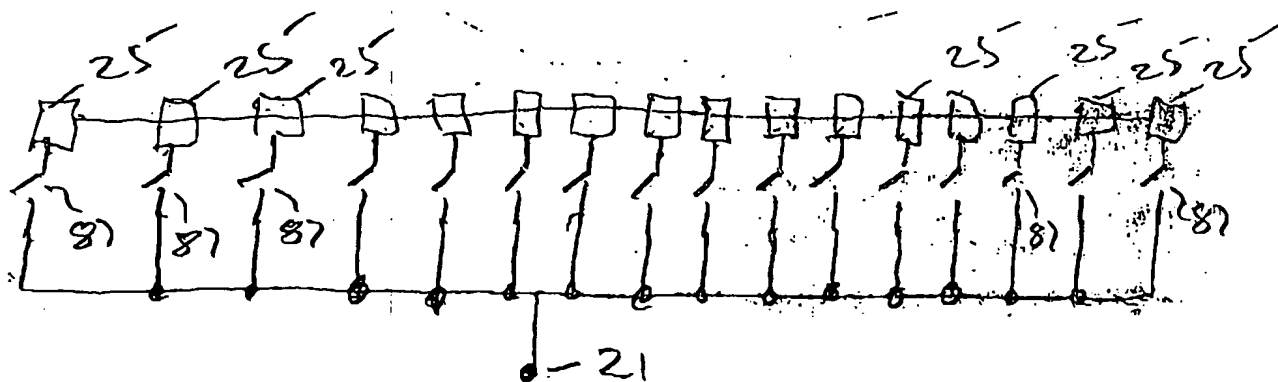


Fig 11



F1G13

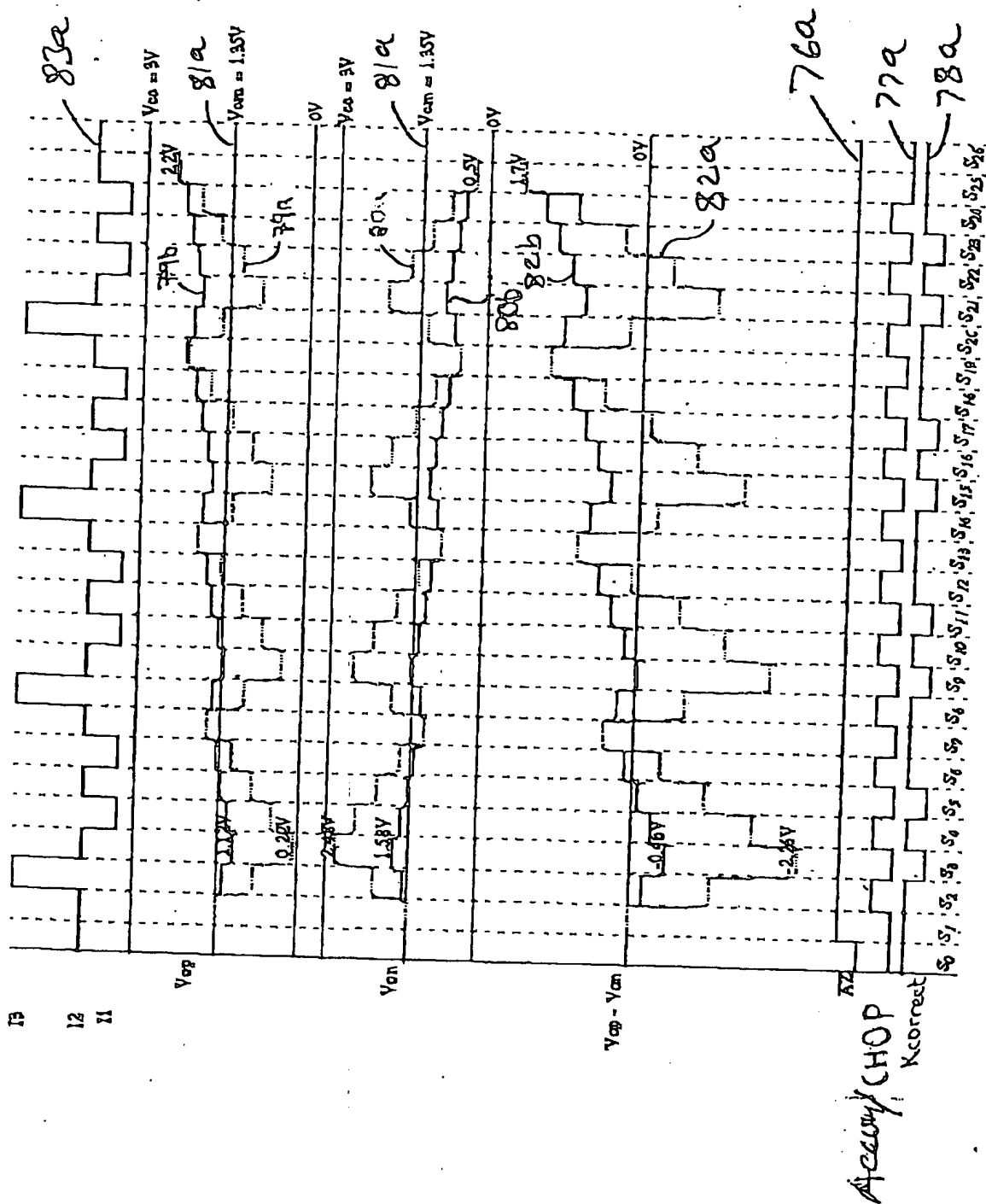


Fig 12

7/8

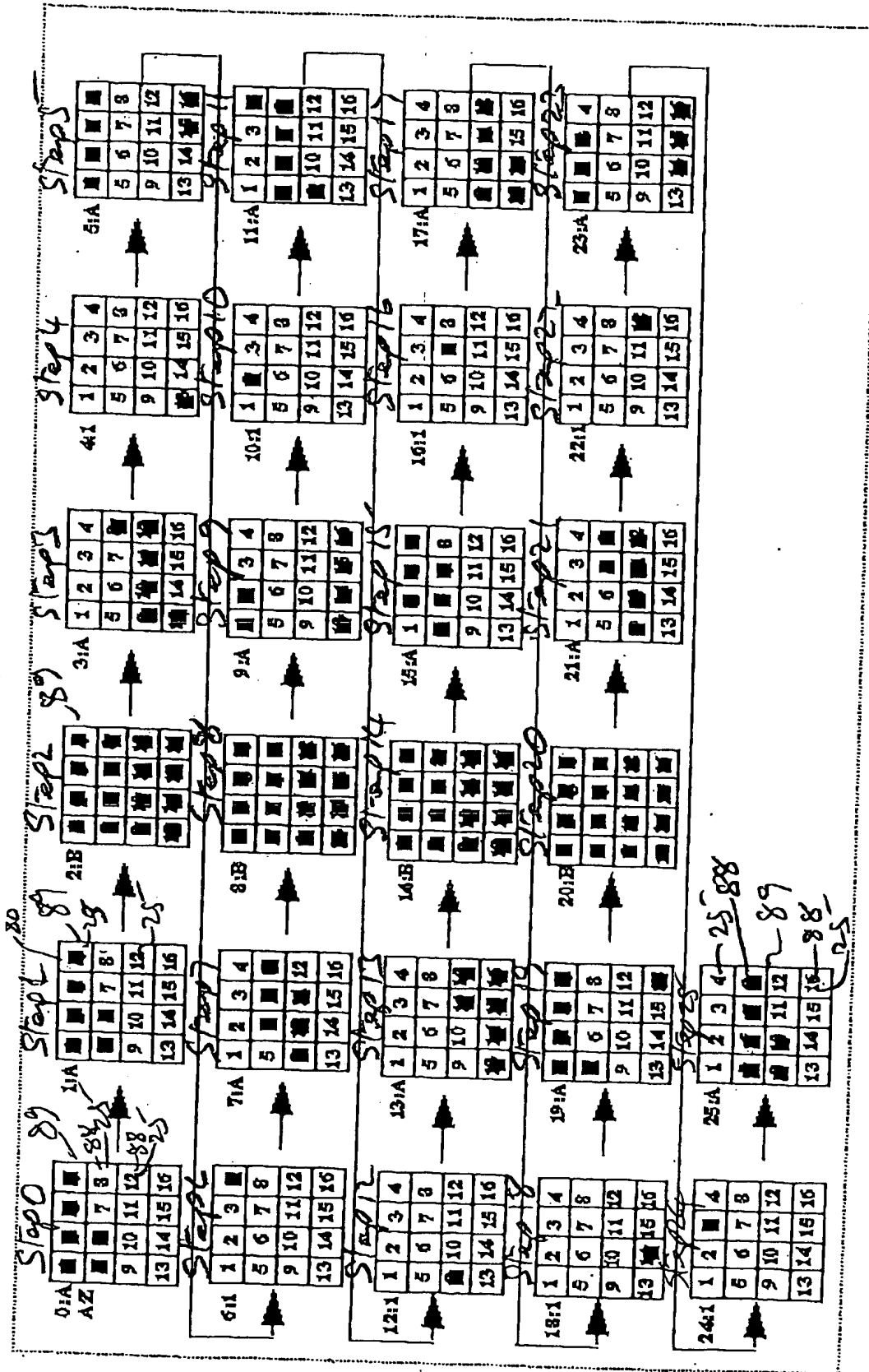
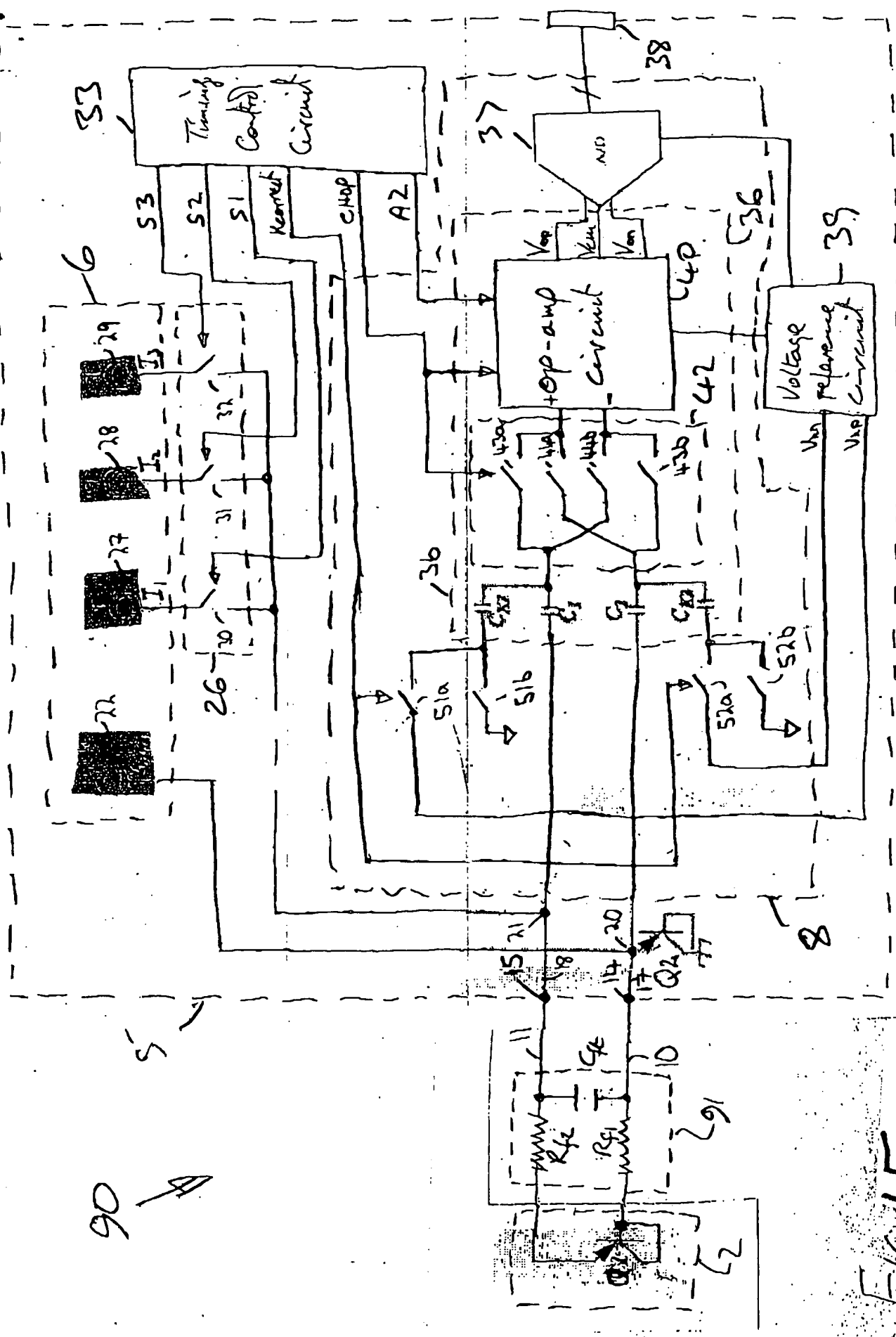


FIG 14



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